WHAT IS CLAIMED IS:

1. A method of processing data based on programmed instructions, the method comprising:

referencing a number of locations in memory by forming addresses and correct buffer mappings corresponding to separate buffers in a plurality of buffers; and

communicating data from the referenced locations in memory to a processing unit, wherein the processing unit concurrently receives inputs from the separate buffers in the plurality of buffers and outputs to another buffer in the plurality of buffers.

2. The method of claim 1, further comprising selectively directing the data from the separate buffers to one processing unit of a plurality of processing units, wherein the one processing unit is configured to perform finite impulse response (FIR) operations.

3. The method of claim 1, further comprising selectively directing the data from the separate buffers to one processing unit of a plurality of processing units, wherein the one processing unit is configured to perform Fast Fourier Transform (FFT) operations.

4. The method of claim 1, further comprising selectively directing the data from the separate buffers to one processing unit of a plurality of processing units, wherein the one processing unit is configured to perform vector processing operations.

5. The method of claim 4, further comprising accumulating results of successive outputs.

6. The method of claim 4, wherein the vector processing operations comprise a single instruction that drives calculation of a vector.

7. The method of claim 1, further comprising a plurality of processing units, the plurality of processing units having power on when in use and power off when not in use.

8. The method of claim 1, further comprising a plurality of processing units, the plurality of processing units having an enabled clock when in use and a disabled clock when not in use.

9. The method of claim 8, wherein the plurality of processing units comprise a first processing unit configured to perform a finite impulse response (FIR) filtering operation, a second processing unit configured to perform Fast Fourier Transform (FFT) operations, and a third processing unit configured to perform vector processing operations.

10. The method of claim 1, wherein communicating data from the referenced locations in memory to a processing unit comprises communicating data to a bit shifting unit configured to shift communicated data bits and communicate the shifted communicated data bits to the processing unit.

11. The method of claim 1, further comprising communicating data from the processing unit to a bit shifting unit configured to shift communicated data bits according to programmed instructions.

12. An apparatus operable to process communication signals, the apparatus comprising:

a plurality of buffers;

a controller including programmed instructions configured to reference a number of locations in memory by forming addresses and correct buffer mappings corresponding to separate buffers in the plurality of buffers; and

a processing unit that concurrently receives inputs from the separate buffers in the plurality of buffers and outputs to another buffer in the plurality of buffers.

13. The apparatus of claim 12, further comprising a plurality of processing units including a first processing unit configured to perform a finite impulse response (FIR) filtering operation, a second processing unit configured to perform Fast Fourier Transform (FFT) operations, and a third processing unit configured to perform vector processing operations.

14. The apparatus of claim 13, wherein the first, second, and third processing units selectively receive signal samples from the plurality of buffers, perform operations on the received signal samples, and communicate results of the performed operations to the plurality of buffers.

15. The apparatus of claim 13, wherein the FIR filtering operation comprises a convolution operation.

16. The apparatus of claim 13, wherein the FFT operations comprise a butterfly operation.

17. A system for processing communication signals communicated, the system comprising:

means for referencing a number of locations in memory by forming addresses and correct buffer mappings corresponding to separate buffers in a plurality of buffers; and

means for communicating data from the referenced locations in memory to a processing unit, wherein the processing unit concurrently receives inputs from the separate buffers in the plurality of buffers and outputs to another buffer in the plurality of buffers.

18. The system of claim 17, further comprising means for selectively directing the received data to any one of (a) means for performing finite impulse response (FIR) operations; (b) means for performing Fast Fourier Transform operations; and (c) means for performing vector processing operations.

19. The system of claim 18, further comprising means for controlling operation states of the means for selectively directing the received data.

20. The system of claim 18, further comprising means for addressing memory buffers configured to receive results from the (a) means for performing pulse shaping operations; (b) means for performing fast Fourier transform operations; and (c) means for performing vector processing operations.

21. The system of claim 17, wherein the received data comprise signal samples that conform to 802.11a protocol specifications.

22. The system of claim 17, wherein the received data comprise signal samples that conform to 802.11g protocol specifications.

23. A method of processing data based on programmed instructions, the method comprising:

performing vector processing operations, wherein the vector processing operations comprise a single instruction that drives calculation of a vector.

24. The method of claim 23, further comprising:

referencing a number of locations in memory by forming addresses and correct buffer mappings corresponding to separate buffers in a plurality of buffers; and

communicating data from the referenced locations in memory to a processing unit, wherein the processing unit concurrently receives inputs from the separate buffers in the plurality of buffers and outputs to another buffer in the plurality of buffers.

25. The method of claim 23, further comprising selectively directing the data from the separate buffers to one processing unit of a plurality of processing units, wherein the one processing unit is configured to perform vector processing operations.

26. A method of processing data based on programmed instructions, the method comprising:

demodulating a 802.11-compliant waveform, wherein the 802.11-compliant waveform is processed asynchronously to a sample rate associated with the waveform and based on programmed instructions in programmed memory.

27. A method of processing data based on programmed instructions, the method comprising:

referencing a number of locations in memory by forming addresses and correct buffer mappings corresponding to separate buffers in a plurality of buffers; and

communicating data from the referenced locations in memory to a processing unit, wherein the processing unit concurrently receives inputs from the separate buffers in the plurality of buffers and outputs to another buffer in the plurality of buffers,

wherein the buffer mappings change such that a buffer mapped as an output is mapped to be an input after an instruction is executed.

28. The method of claim 27, further comprising a second processing unit wherein the second processing unit maps a particular buffer as an output and the particular buffer is mapped as an input to the processing unit after the instruction is executed.